Fig.1

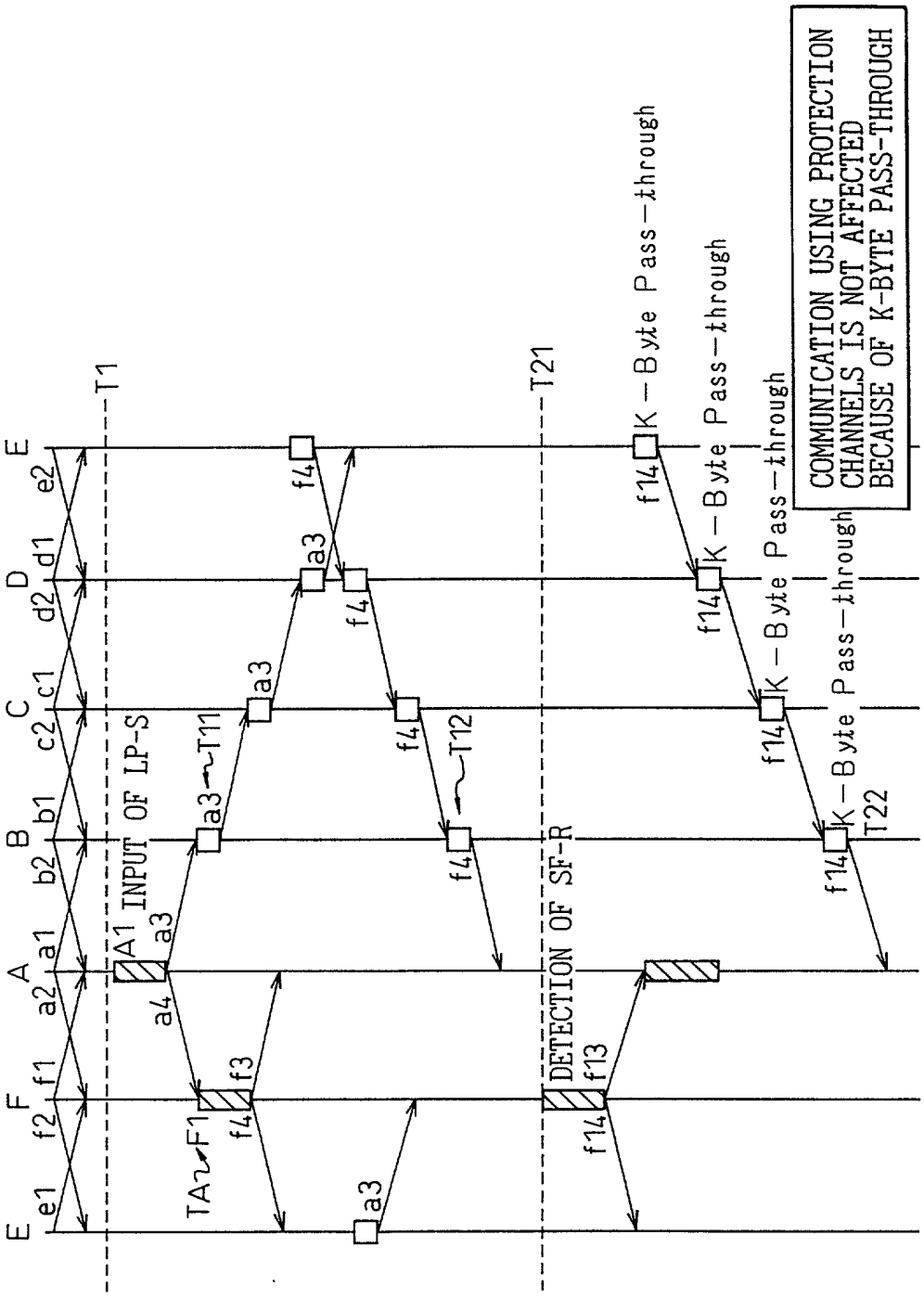

E
e1
F
f2
f1
A
a2
a1
B
b2
b1
C
c2
c1
D
d2
d1
E
e2
T1
T21
A1 INPUT OF LP-S
a3
a4
TA~F1
f3
f4
a3~T11
T11
a3
f4
f4
a3
f4
~T12
T12
f4
DETECTION OF SF-R
f13
f14
f14
K-Byte Pass-through
f14
K-Byte Pass-through
f14
K-Byte Pass-through
f14
K-Byte Pass-through
T22
COMMUNICATION USING PROTECTION CHANNELS IS NOT AFFECTED BECAUSE OF K-BYTE PASS-THROUGH

Fig.2

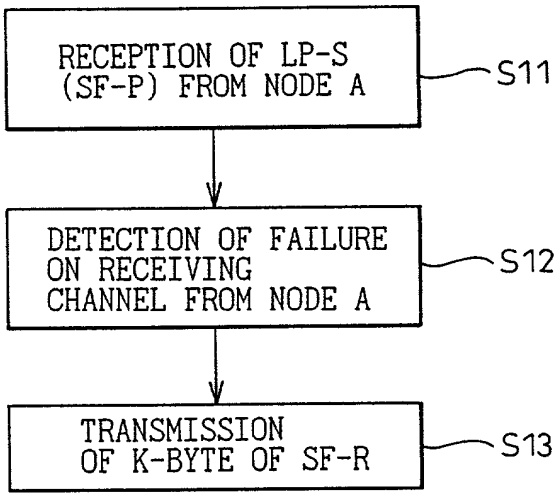

RECEPTION OF LP-S (SF-P) FROM NODE A
S11
DETECTION OF FAILURE ON RECEIVING CHANNEL FROM NODE A
S12
TRANSMISSION OF K-BYTE OF SF-R
S13

Fig.3

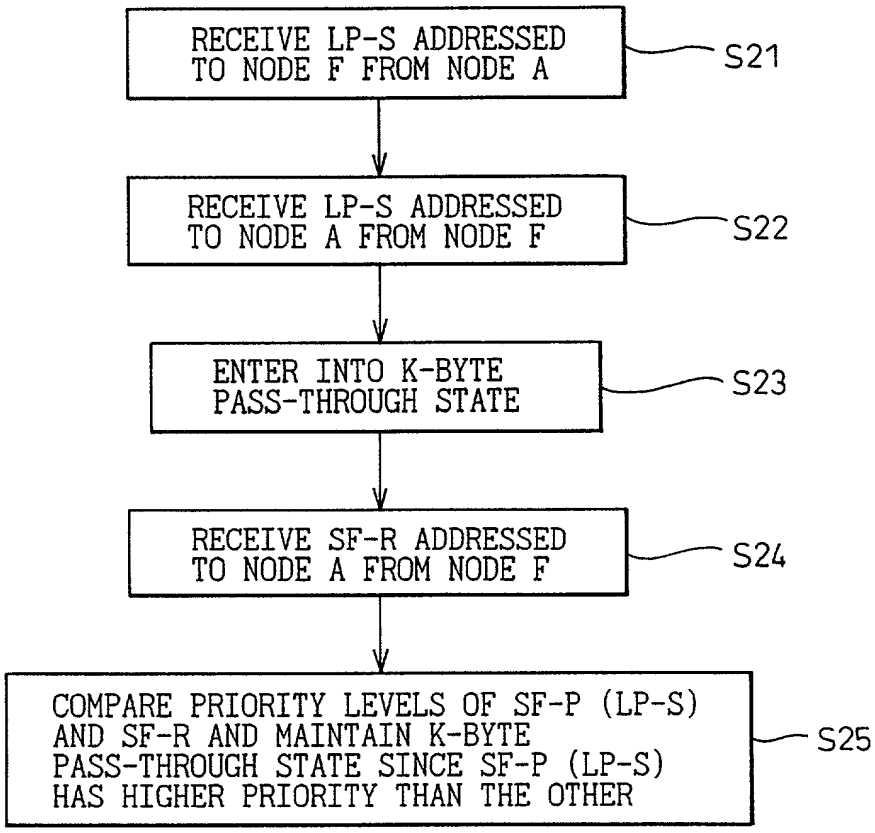

RECEIVE LP-S ADDRESSED TO NODE F FROM NODE A
S21
RECEIVE LP-S ADDRESSED TO NODE A FROM NODE F
S22
ENTER INTO K-BYTE PASS-THROUGH STATE
S23
RECEIVE SF-R ADDRESSED TO NODE A FROM NODE F
S24
COMPARE PRIORITY LEVELS OF SF-P (LP-S) AND SF-R AND MAINTAIN K-BYTE PASS-THROUGH STATE SINCE SF-P (LP-S) HAS HIGHER PRIORITY THAN THE OTHER
S25

Fig.4

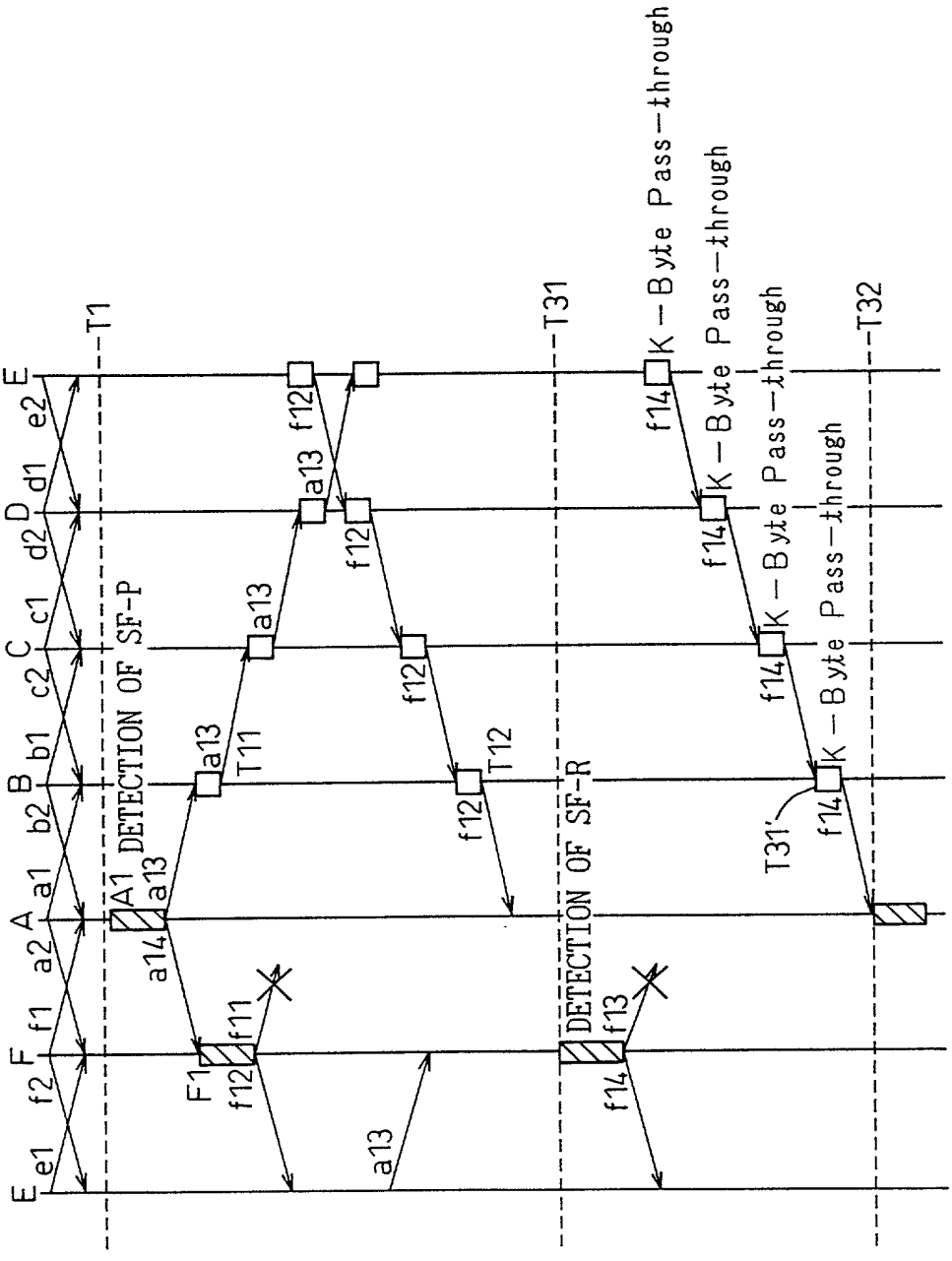

E
F
A
B
C
D
E
e1
f2
f1
a2
a1
b2
b1
c2
c1
d2
d1
e2
T1
T31
T32
T11
T12
T31'
A1
DETECTION OF SF-P
DETECTION OF SF-R
F1
a13
a14
f11
f12
f13
f14
K - Byte Pass-through

Fig.5

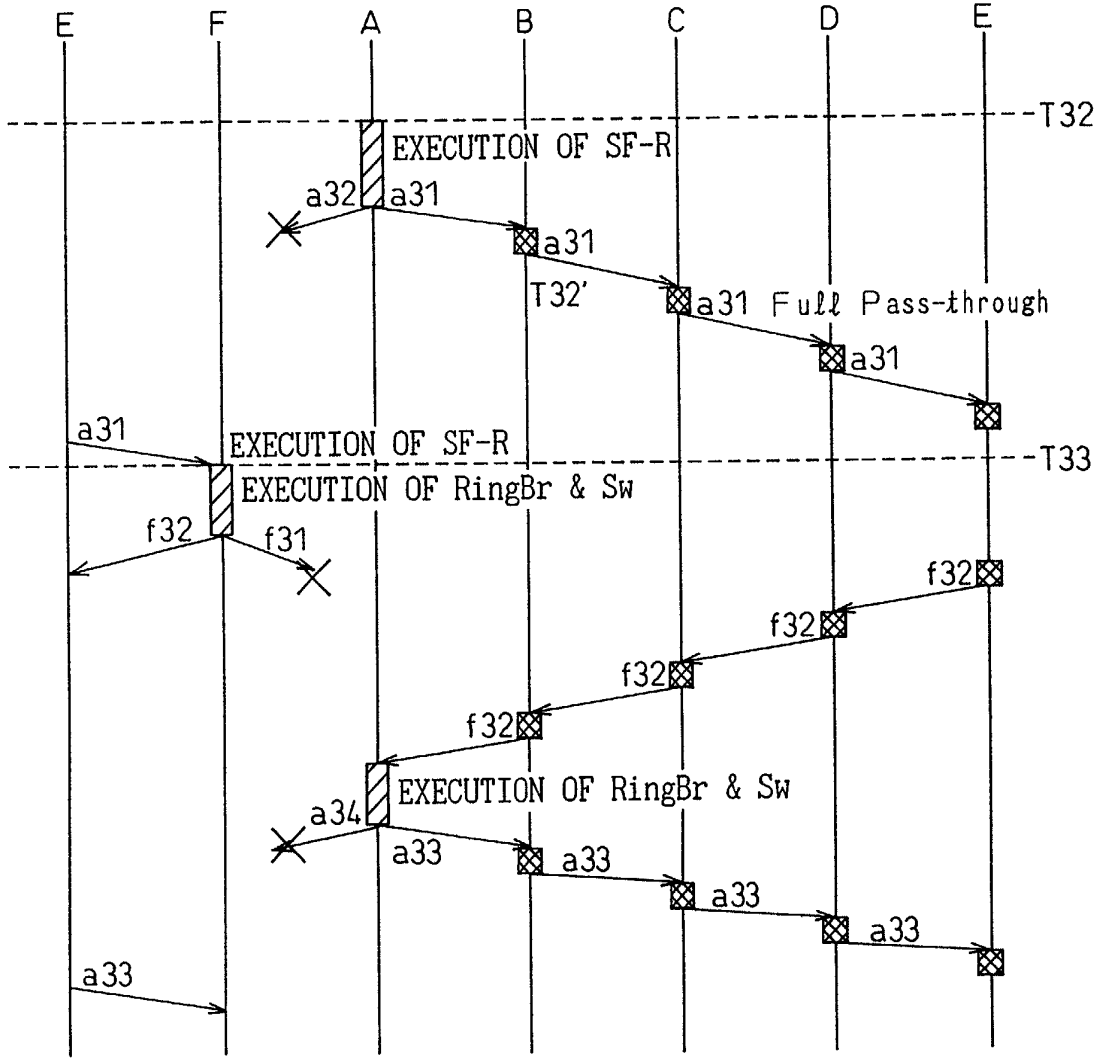
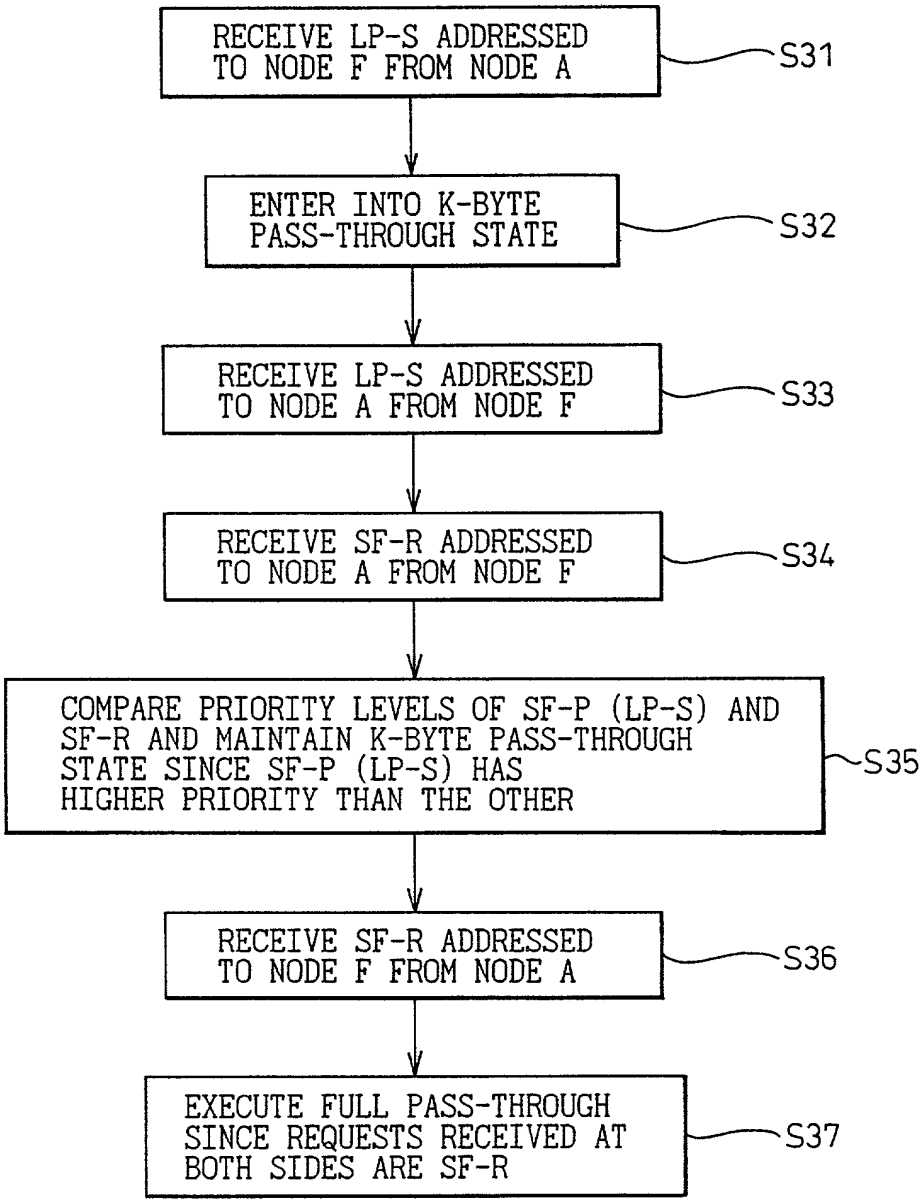

E
F
A
B
C
D
E
T32
EXECUTION OF SF-R
a32
a31
a31
T32'
a31 Full Pass-through
a31
a31
EXECUTION OF SF-R
T33
EXECUTION OF RingBr & Sw
f32
f31
f32
f32
f32
f32
EXECUTION OF RingBr & Sw
a34
a33
a33
a33
a33
a33

Fig.6


RECEIVE LP-S ADDRESSED TO NODE F FROM NODE A
S31
ENTER INTO K-BYTE PASS-THROUGH STATE
S32
RECEIVE LP-S ADDRESSED TO NODE A FROM NODE F
S33
RECEIVE SF-R ADDRESSED TO NODE A FROM NODE F
S34
COMPARE PRIORITY LEVELS OF SF-P (LP-S) AND SF-R AND MAINTAIN K-BYTE PASS-THROUGH STATE SINCE SF-P (LP-S) HAS HIGHER PRIORITY THAN THE OTHER
S35
RECEIVE SF-R ADDRESSED TO NODE F FROM NODE A
S36
EXECUTE FULL PASS-THROUGH SINCE REQUESTS RECEIVED AT BOTH SIDES ARE SF-R
S37

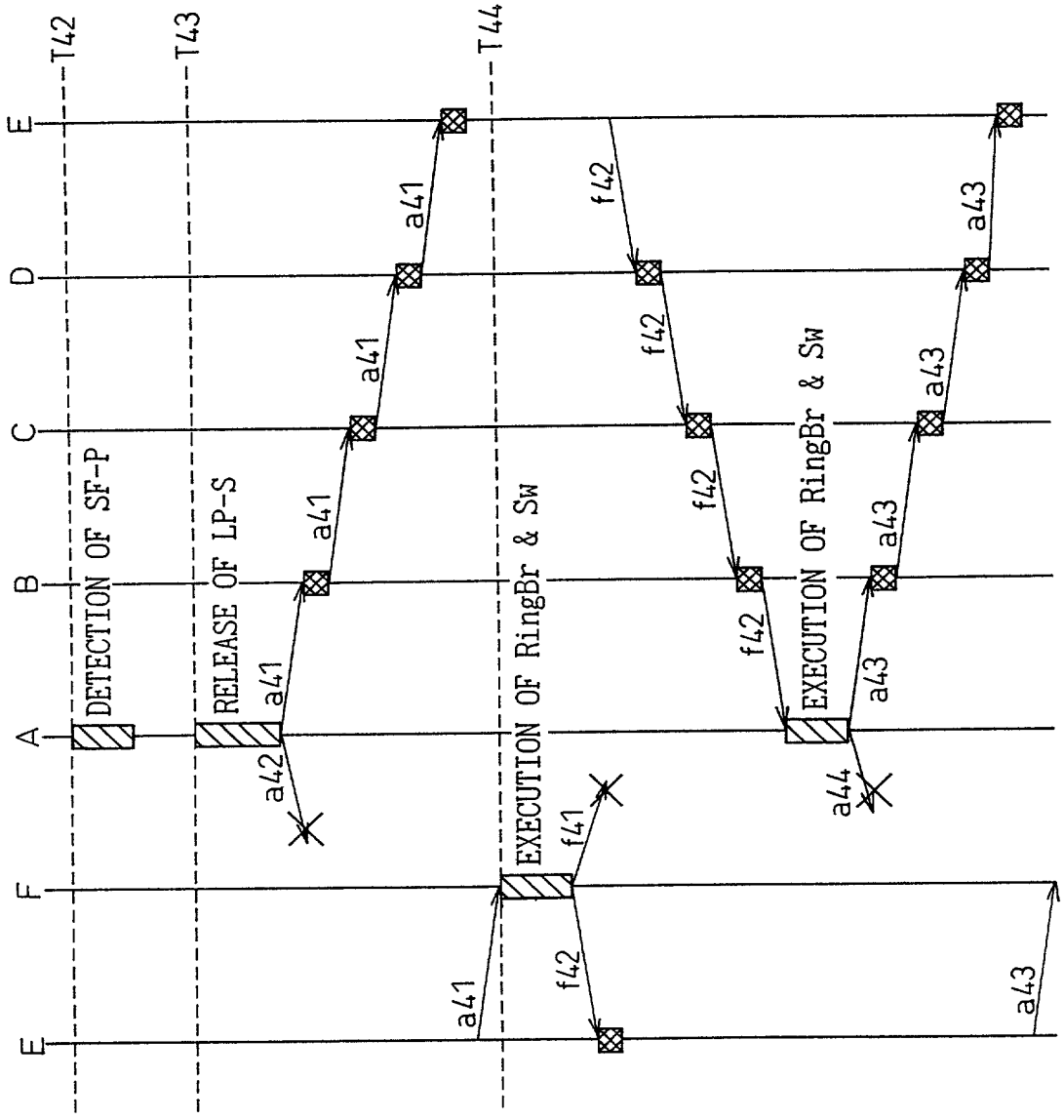

T42
T43
T44
A
B
C
D
E
F
E
DETECTION OF SF-P
RELEASE OF LP-S
EXECUTION OF RingBr & Sw
EXECUTION OF RingBr & Sw
a41
a41
a41
a42
a41
f42
f42
f42
f42
a43
a43
a43
a44
f41
f42
a43

Fig.7

Fig.8

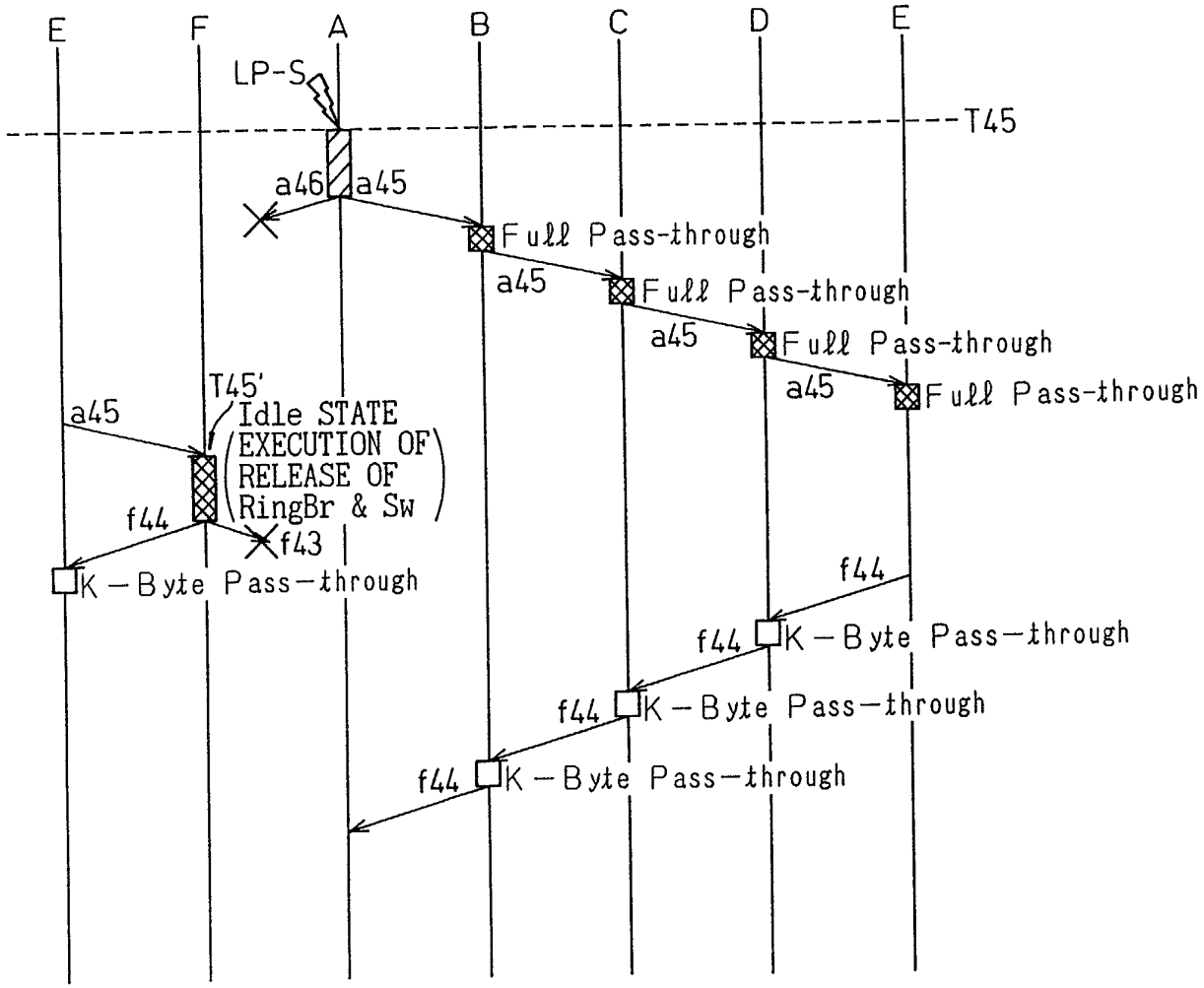
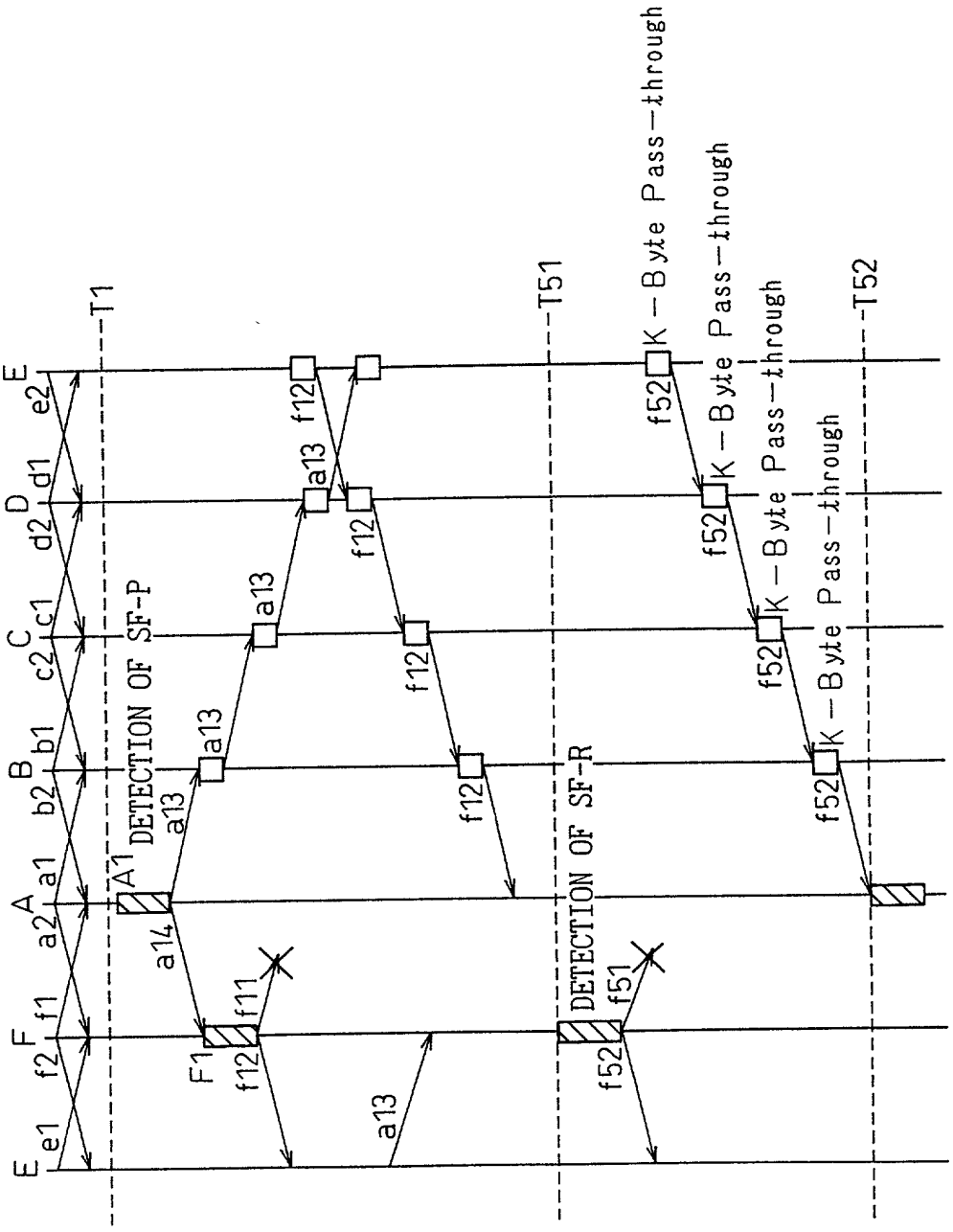

E
F
A
B
C
D
E
LP-S
T45
a46
a45
Full Pass-through
a45
Full Pass-through
a45
Full Pass-through
a45
Full Pass-through
T45'
Idle STATE
EXECUTION OF
RELEASE OF
RingBr & Sw
a45
f44
f43
K-Byte Pass-through
f44
f44
K-Byte Pass-through
f44
K-Byte Pass-through
f44
K-Byte Pass-through

Fig.9


T1
T51
T52
E
D
C
B
A
F
e1
e2
d1
d2
c1
c2
b1
b2
a1
a2
f1
f2
A1
DETECTION OF SF-P
DETECTION OF SF-R
a13
a14
f11
f12
F1
f51
f52
K-Byte Pass-through

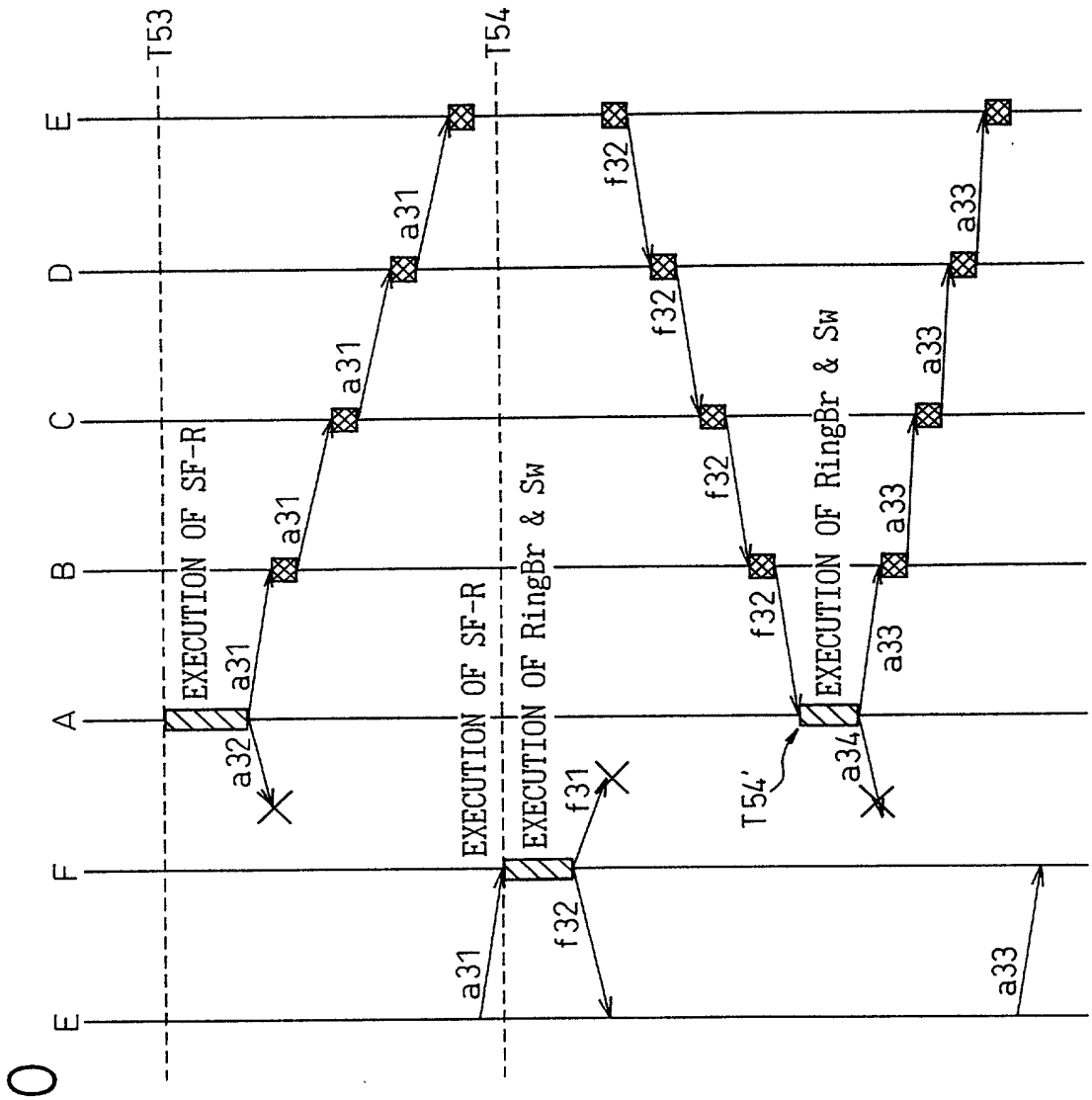

T53
T54
A
B
C
D
E
F
E
EXECUTION OF SF-R
a31
a31
a31
a31
a32
EXECUTION OF SF-R
EXECUTION OF RingBr & Sw
f31
f32
a31
f32
f32
f32
f32
EXECUTION OF RingBr & Sw
T54'
a34
a33
a33
a33
a33
a33

Fig.10

Fig.11

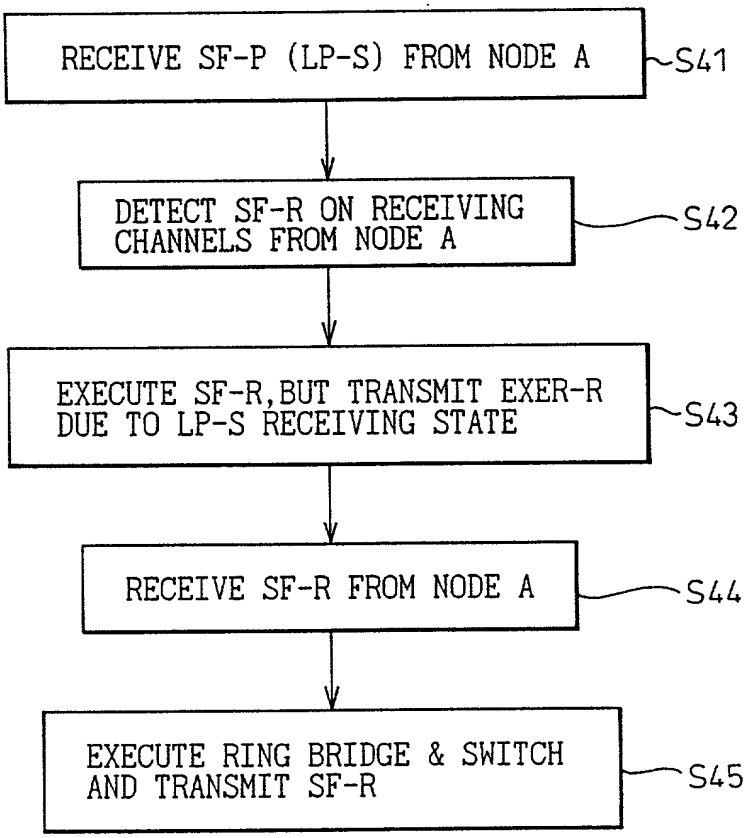

RECEIVE SF-P (LP-S) FROM NODE A
S41
DETECT SF-R ON RECEIVING CHANNELS FROM NODE A
S42
EXECUTE SF-R,BUT TRANSMIT EXER-R DUE TO LP-S RECEIVING STATE
S43
RECEIVE SF-R FROM NODE A
S44
EXECUTE RING BRIDGE & SWITCH AND TRANSMIT SF-R
S45

Fig.12

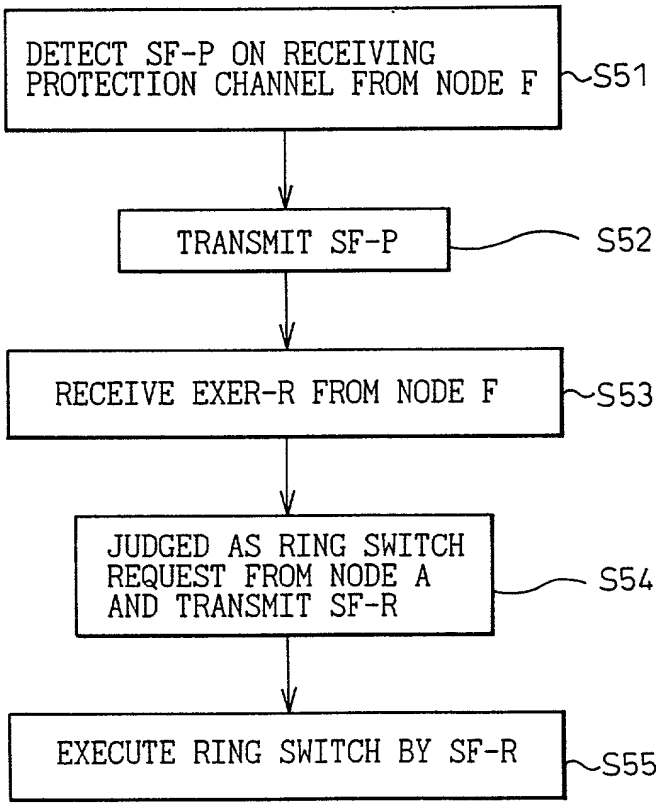

DETECT SF-P ON RECEIVING PROTECTION CHANNEL FROM NODE F
S51
TRANSMIT SF-P
S52
RECEIVE EXER-R FROM NODE F
S53
JUDGED AS RING SWITCH REQUEST FROM NODE A AND TRANSMIT SF-R
S54
EXECUTE RING SWITCH BY SF-R
S55

Fig.13

K1Byte	K2Byte	MEANING
Bit1-4	Bit6-8	
SF-P(LP-S)	100	LP-S(Idle)
SF-P(LP-S)	101	LP-S (STATE EXCEPT FOR Idle)
SF-P(LP-S)	EXCEPT FOR 100,101	SF-P (INTERPRET AS MEANING OF K2 Byte Bit6-8 DEFINED BY GR1230-CORE)

Fig.14

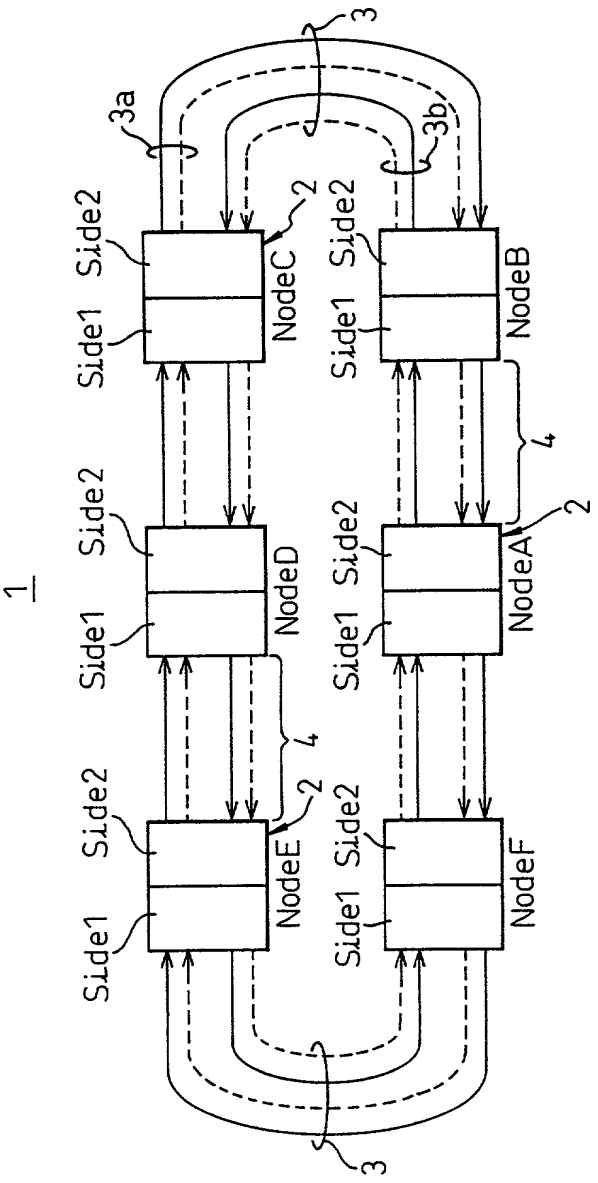


Fig.15

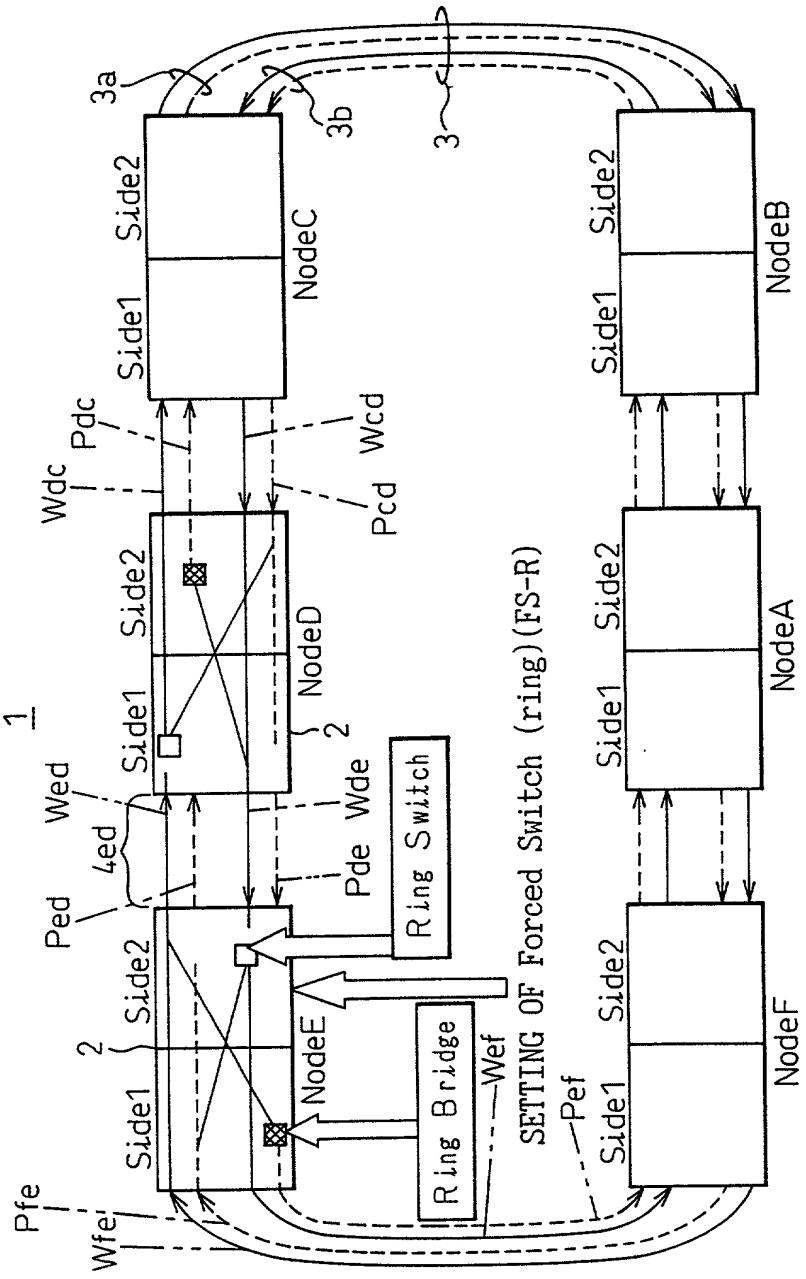

1
3a
3b
3
NodeC
NodeB
NodeD
NodeA
NodeE
NodeF
Side1
Side2
Wdc
Pdc
Wcd
Pcd
Wed
Ped
4ed
Pde
Wde
Ring Switch
Ring Bridge
Wef
Pef
Pfe
Wfe
SETTING OF Forced Switch (ring)(FS-R)

Fig.16

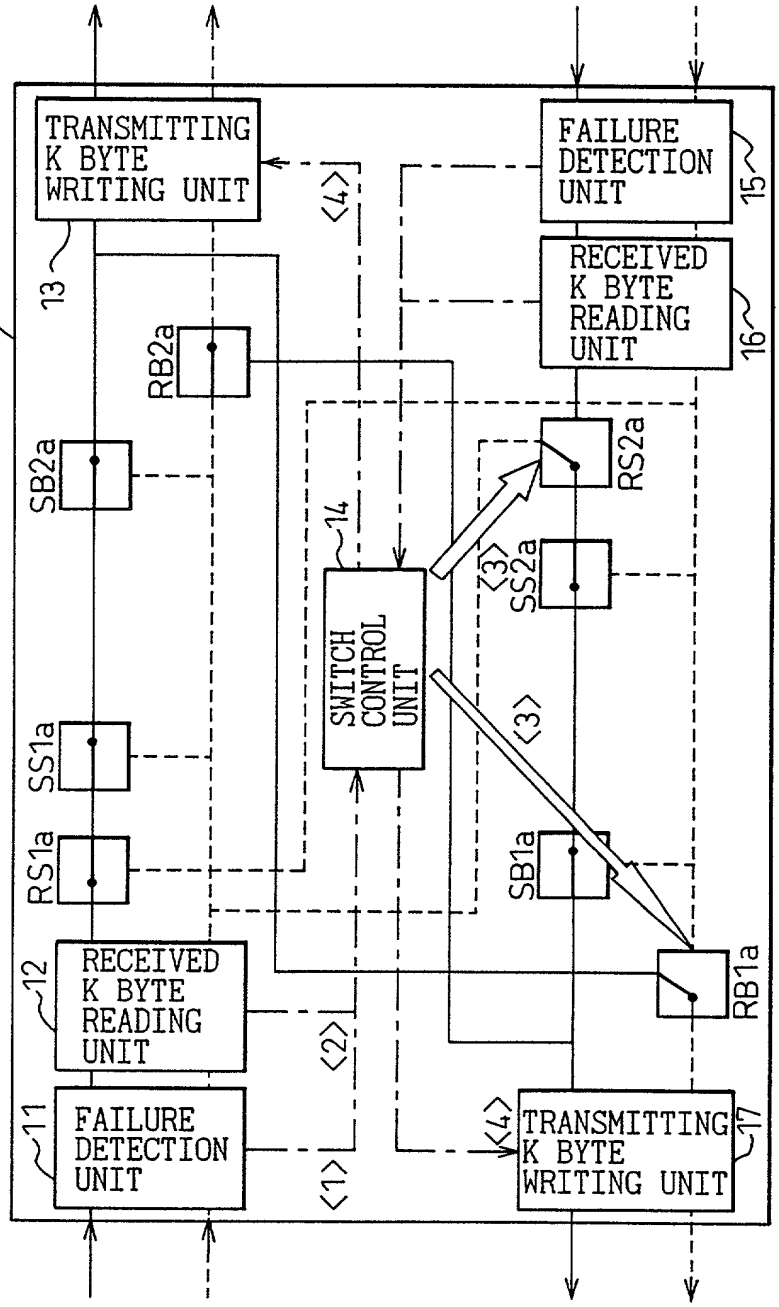

TRANSMITTING K BYTE WRITING UNIT
13
2
FAILURE DETECTION UNIT
15
RECEIVED K BYTE READING UNIT
16
RB2a
SB2a
RS2a
SS2a
14
SWITCH CONTROL UNIT
SS1a
RS1a
SB1a
RB1a
RECEIVED K BYTE READING UNIT
12
FAILURE DETECTION UNIT
11
TRANSMITTING K BYTE WRITING UNIT
17
<1>
<2>
<3>
<4>

Fig.17

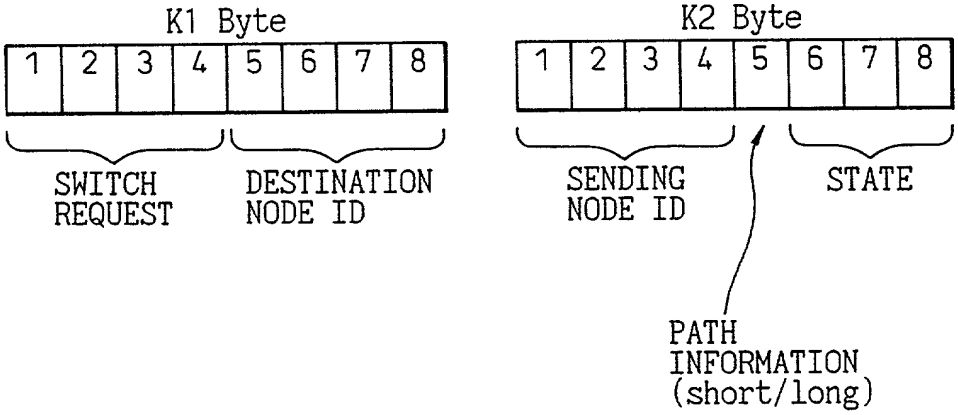

K1 Byte
1
2
3
4
5
6
7
8
SWITCH REQUEST
DESTINATION NODE ID
K2 Byte
1
2
3
4
5
6
7
8
SENDING NODE ID
STATE
PATH INFORMATION (short/long)

Fig.18

SWITCH REQUEST		
BIT 1 ~ BIT 4	BIT	PRIORITY LEVELS
	1111	Lockout of Protection (span) [LP−S] or Signal Fail (protection) [SF−P]
	1110	Forced Switch (span) [FS−S]
	1101	Forced Switch (ring) [FS−R]
	1100	Signal Fail (span) [SF−S]
	1011	Signal Fail (ring) [SF−R]
	1010	Signal Degrade (protection) [SD−P]
	1001	Signal Degrade (span) [SD−S]
	1000	Signal Degrade (ring) [SD−R]
	0111	Manual Switch (span) [MS−S]
	0110	Manual Switch (ring) [MS−R]
	0101	Wait To Restore [WTR]
	0100	Exerciser (span) [EXER−S]
	0011	Exerciser (ring) [EXER−R]
	0010	Reverse Request (span)[b] [RR−S]
	0001	Reverse Request (ring)[b] [RR−R]
	0000	No Request [NR]

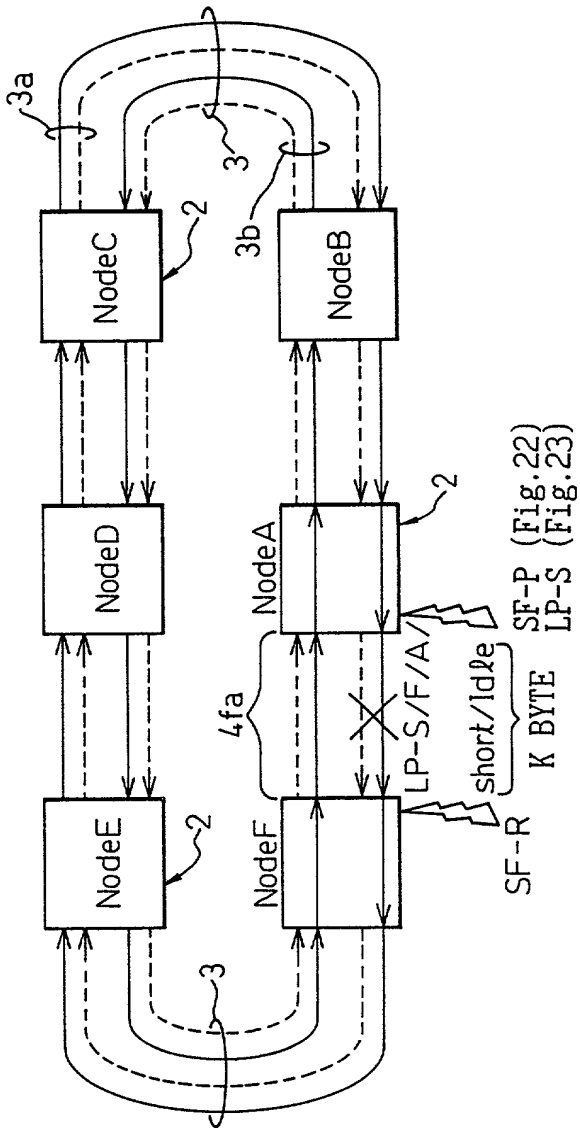
Fig.19

SYMBOL	K1Byte		K2Byte		
	Bit(1-4)	Bit(5-8)	Bit(1-4)	Bit(5)	Bit(6-8)
a1	NR	B	A	short	Idle
a2	NR	F	A	short	Idle
a3	SF-P(LP-S)	F	A	long	Idle
a4	SF-P(LP-S)	F	A	short	RDI
a5	LP-S(SF-P)	F	A	long	Idle
a6	LP-S(SF-P)	F	A	short	Idle
a11	LP-S(SF-P)	F	A	long	Idle
a12	LP-S(SF-P)	F	A	short	Idle
a13	SF-P(LP-S)	F	A	long	Idle
a14	SF-P(LP-S)	F	A	short	RDI
a15	SF-R	F	A	long	Br&Sw
a16	SF-P(LP-S)	F	A	short	Br&Sw
a31	SF-R	F	A	long	Idle
a32	SF-P(LP-S)	F	A	short	RDI
a33	SF-R	A	F	long	Br&Sw
a34	SF-P(LP-S)	A	F	short	RDI
a41	SF-R	F	A	long	Idle
a42	SF-P(LP-S)	F	A	short	RDI
a43	SF-R	F	A	long	Br&Sw
a44	SF-P(LP-S)	F	A	short	RDI
a45	LP-S(SF-P)	F	A	long	Idle
a46	LP-S(SF-P)	F	A	short	RDI
b1	NR	C	B	short	Idle
b2	NR	A	B	short	Idle
c1	NR	D	C	short	Idle
c2	NR	B	C	short	Idle
d1	NR	E	D	short	Idle
d2	NR	C	D	short	Idle

Fig.20

SYMBOL	K1Byte		K2Byte		
	Bit(1-4)	Bit(5-8)	Bit(1-4)	Bit(5)	Bit(6-8)
e1	NR	F	E	short	Idle
e2	NR	D	E	short	Idle
f1	NR	A	F	short	Idle
f2	NR	E	F	short	Idle
f3	RR-S	A	F	short	Idle
f4	LP-S(SF-P)	A	F	long	Idle
f11	RR-S	A	F	short	Idle
f12	SF-P(LP-S)	A	F	long	Idle
f13	SF-R	A	F	short	RDI
f14	SF-R	A	F	long	Idle
f15	SF-R	A	F	short	RDI
f16	SF-R	A	F	long	Br&Sw
f31	SF-R	A	F	short	RDI
f32	SF-R	A	F	long	Br&Sw
f41	SF-R	A	F	short	RDI
f42	SF-R	A	F	long	Br&Sw
f43	SF-R	A	F	short	RDI
f44	SF-R	A	F	long	Idle
f51	EXER-R	A	F	short	RDI
f52	EXER-R	A	F	long	Idle

Fig.21


1
3a
3
3b
NodeC
NodeB
NodeD
NodeA
NodeE
NodeF
2
4fa
LP-S/F/A
short/Idle
K BYTE
SF-R
SF-P (Fig.22)
LP-S (Fig.23)

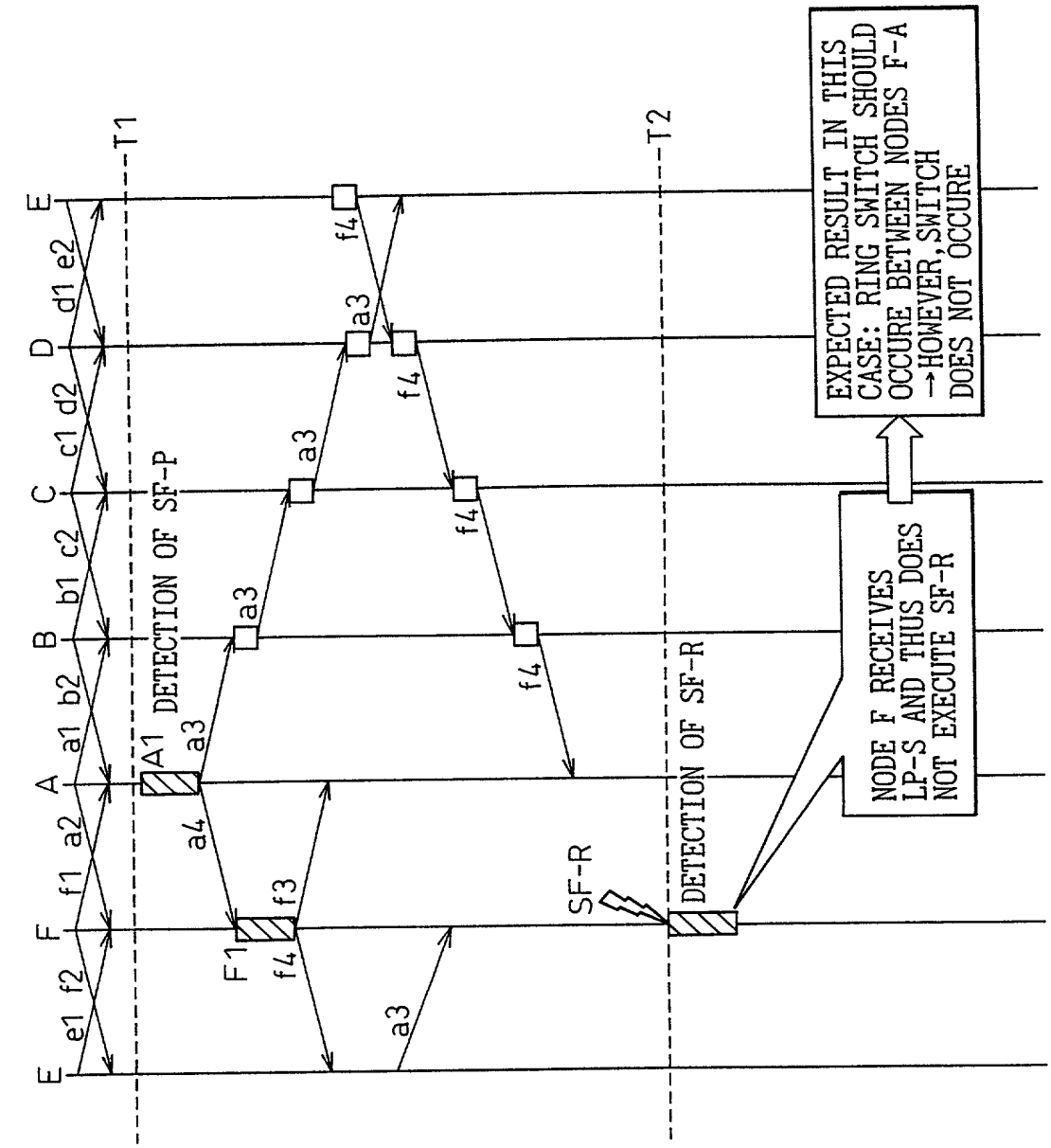

T1
T2
E
D
C
B
A
F
E
e1 f2
f1 a2
a1 b2
b1 c2
c1 d2
d1 e2
A1
DETECTION OF SF-P
F1
SF-R
DETECTION OF SF-R
a3
a4
f3
f4
EXPECTED RESULT IN THIS CASE: RING SWITCH SHOULD OCCURE BETWEEN NODES F-A →HOWEVER,SWITCH DOES NOT OCCURE
NODE F RECEIVES LP-S AND THUS DOES NOT EXECUTE SF-R

Fig.22

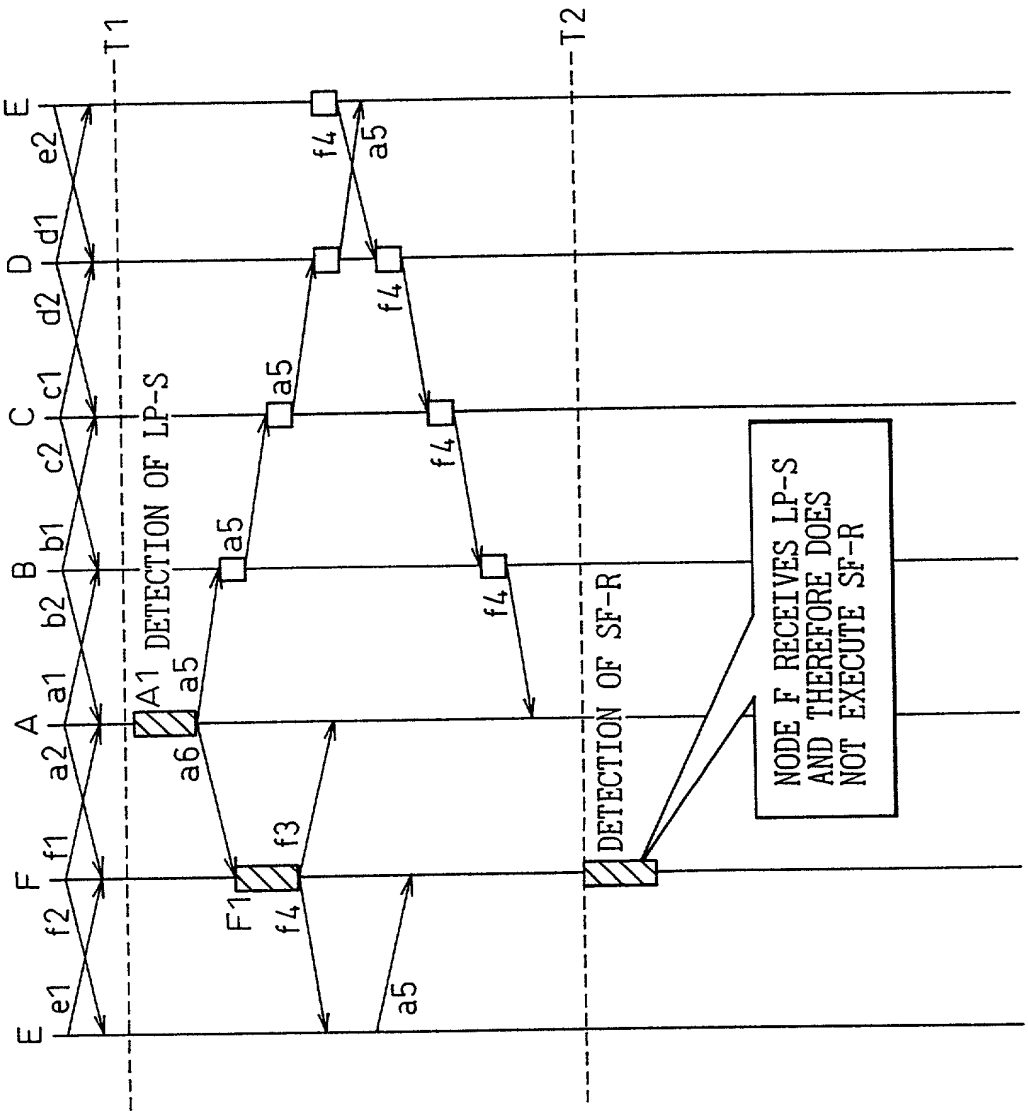

T1
T2
A
B
C
D
E
F
a1
a2
b1
b2
c1
c2
d1
d2
e1
e2
f1
f2
A1
DETECTION OF LP-S
a5
a6
f3
f4
F1
DETECTION OF SF-R
NODE F RECEIVES LP-S
AND THEREFORE DOES
NOT EXECUTE SF-R

Fig.23

Fig. 24

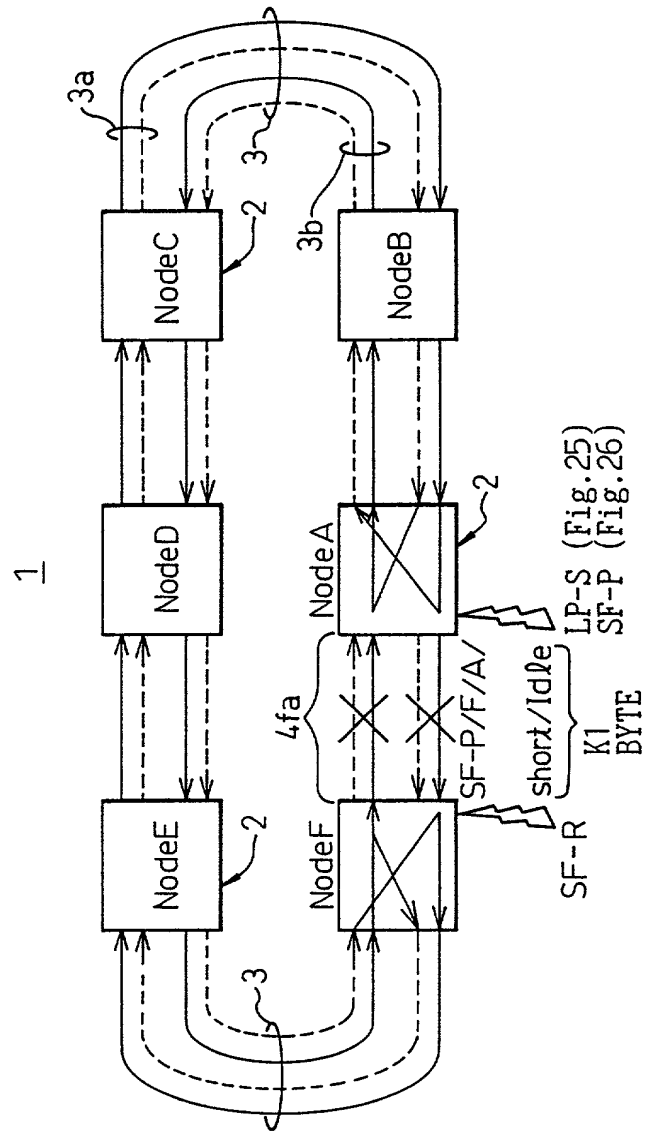

1
3a
3
3b
NodeC
NodeB
NodeD
NodeA
NodeE
NodeF
2
2
2
4fa
SF-P/F/A/
short/Idle
K1
BYTE
LP-S (Fig.25)
SF-P (Fig.26)
SF-R

Fig.25

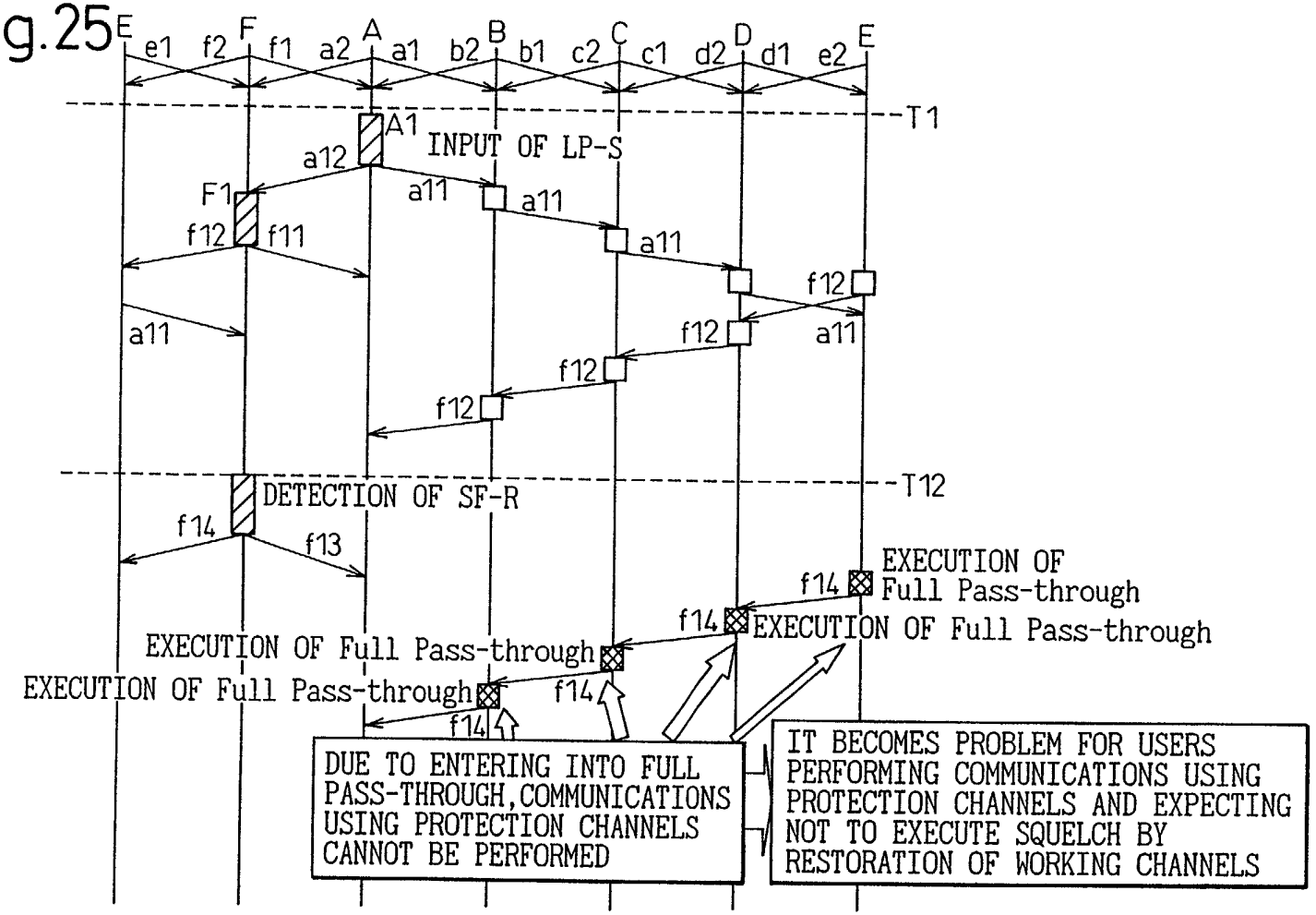
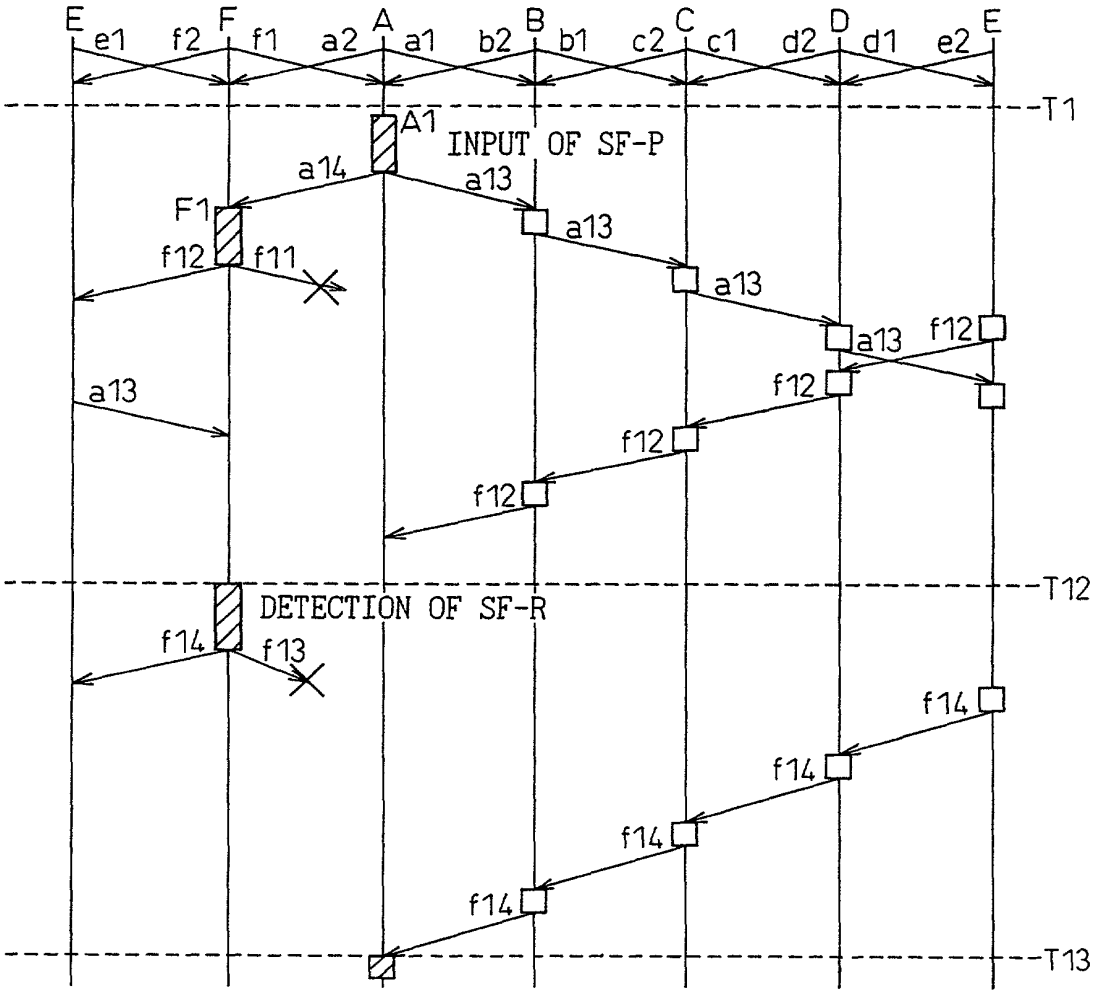

E
e1
f2
F
f1
a2
A
a1
b2
B
b1
c2
C
c1
d2
D
d1
e2
E
T1
A1
INPUT OF LP-S
a12
F1
a11
a11
a11
f12
f11
f12
a11
f12
a11
f12
f12
T12
DETECTION OF SF-R
f14
f13
EXECUTION OF
Full Pass-through
f14
EXECUTION OF Full Pass-through
f14
EXECUTION OF Full Pass-through
EXECUTION OF Full Pass-through
f14
f14
DUE TO ENTERING INTO FULL PASS-THROUGH, COMMUNICATIONS USING PROTECTION CHANNELS CANNOT BE PERFORMED
IT BECOMES PROBLEM FOR USERS PERFORMING COMMUNICATIONS USING PROTECTION CHANNELS AND EXPECTING NOT TO EXECUTE SQUELCH BY RESTORATION OF WORKING CHANNELS

Fig.26


E
e1
f2
F
f1
a2
A
a1
b2
B
b1
c2
C
c1
d2
D
d1
e2
E
T1
A1
INPUT OF SF-P
a14
a13
F1
f12
f11
a13
a13
a13
f12
f12
a13
f12
f12
T12
DETECTION OF SF-R
f14
f13
f14
f14
f14
f14
T13

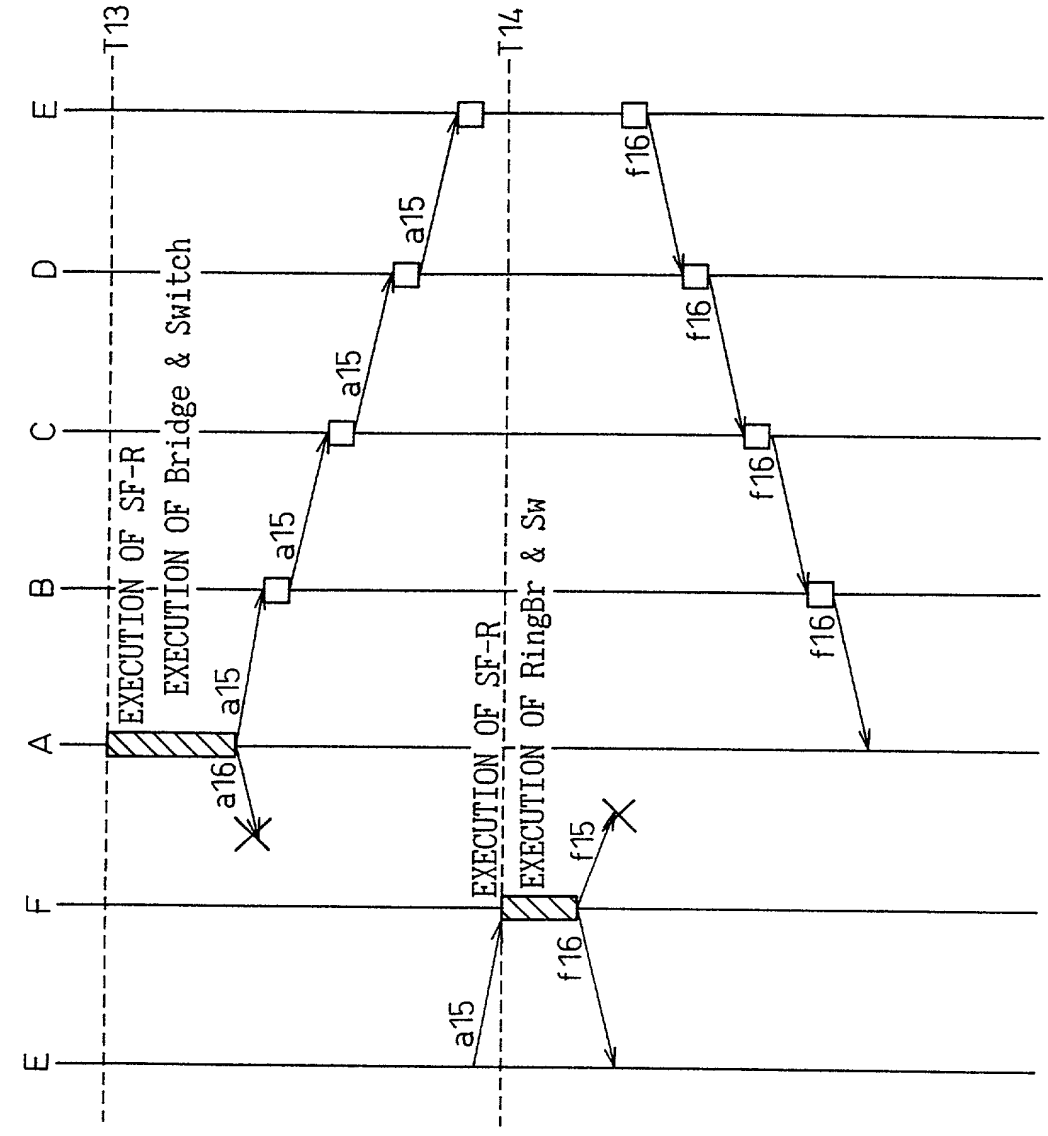

T13
T14
E
D
C
B
A
F
E
EXECUTION OF SF-R
EXECUTION OF Bridge & Switch
EXECUTION OF SF-R
EXECUTION OF RingBr & Sw
a15
a15
a15
a16
a15
f16
f16
f16
f16
f15
f16

Fig.27